[0016] In practice, however, not only the depression type FET but also a so-called enhancement type FET, where drain current cannot flow when the gate bias is zero but flows as the gate bias is applied, are needed.

[0017] However, as the enhancement type FET made of nitride semiconductor is not available at present and there are many restrictions on the design of circuit placing limitations on the applications thereof, there has been a strong demand for the enhancement type FET made of nitride semiconductor.

[0018] In order to manufacture the enhancement type FET, it is necessary to control the formation of the inversion layer in the nitride semiconductor layer structure.

[0019] In an FET made of an arsenide semiconductor, for example, formation of the inversion layer can be controlled by keeping the thickness of a barrier layer formed from aluminum gallium arsenide within several tens of nanometers, thus making it possible to selectively manufacture the depression type and the enhancement type FETs.

[0020] While the design of a circuit may require the depression type FET, which needs two power supplies of positive and negate voltages in order to operate, it results in such problems as increased power consumption and larger number of components in the circuit that uses it.

[0021] As described above, the piezoelectric field of the nitride semiconductor has a significant influence on the characteristics of the semiconductor device. Japanese Journal of Applied Physics, Vol. 39 (2000), pp 413-416 reports a method for growing crystal that is free from the problem of piezoelectric field, which is accomplished through (11-20) orientation (hereinafter referred to as A axis orientation) or (10-10) orientation.

[0022] While there is no effective way to grow a nitride semiconductor with (10-10) orientation, Japanese Journal of Applied Physics, Vol. 42 (2003), L818-L820 describes a method of using (01-12) sapphire substrate (hereinafter referred to as R-plane sapphire substrate) and Applied Physics Letters, Vol. 83 (2003), pp 5208-5210 describes a method of growing AlN on 4H—SiC (11-20) substrate, for growing a nitride semiconductor with **(10-20)** orientation. Among these, the latter is not practical since it is difficult to obtain large 4H—SiC (11-20) substrate with the current manufacturing techniques and the method is not suited for volume production. The R-plane sapphire substrate, in contrast, can be manufactured to a size of 8 inches at present, thus eliminating the problem of substrate size. In addition, this method is very promising for industrial applications, since it can be carried out in a semiconductor device manufacturing process similar to that of manufacturing silicon-based semiconductor devices, and it can be applied in combination with an SOS (silicon-on-sapphire) device. Accordingly, it is considered to be most advantageous to employ the method of growing the nitride semiconductor on R-plane sapphire substrate, from the view point of volume production and manufacturing cost.

[0023] Through researches conducted by the inventors of the present application and others, it has been found that growing the nitride semiconductor on R-plane sapphire substrate has such problems that much threading dislocations and stacking faults are introduced into the crystal due to a large difference in the lattice constant and non-polarity of sapphire, and that unfavorable form of crystal is involved that makes it difficult to form a steep interface that is required to manufacture the semiconductor device.

[0024] As the means for reducing the density of threading dislocations, in has been reported in Applied Physics Letters, Vol. 84 (2004), pp 3663-3665 to increase the thickness of the GaN layer. As shown in **FIG. 20**, an n-type GaN layer **125** having thickness of 30 μm, an n-type $Al_{0.1}Ga_{0.9}N$ cladding layer **126**, a $GaN/In_{0.15}Ga_{0.85}N$ active layer of multiple quantum well structure **127**, a p-type $Al_{0.1}Ga_{0.9}N$ cladding layer **128** and a p-type GaN layer **129** are formed successively on the R-plane sapphire substrate **11** by the MOVPE method. Then the n-type GaN layer **125** is exposed by dry etching, whereon a p-side electrode **130** and an n-side electrode **131** are formed, thereby to obtain the light emitting diode **137**.

[0025] Another method of reducing the density of threading dislocations that utilizes selective growth in lateral direction is described in Applied Physics Letters, Vol. 81 (2002), pp 1201-1203. As shown in **FIG. 21**, after growing a GaN layer **132** by the MOVPE method on the R-plane sapphire substrate **11**, a mask **133** is formed from SiO_2 by known techniques of photolithography and wet etching, followed by regrowth of GaN layer **134** by the MOVPE method. With this method, the mask **133** prevents the threading dislocations from propagating to the regrowth layer, thus reducing the density of threading dislocations.

[0026] Although the method described in Applied Physics Letters, Vol. 84 (2004), pp 3663-3665 is useful in that consideration is given to the piezoelectric field in the active layer **127**, it is not suited for practical applications because of such problems as the n-type GaN layer **125** having thickness of 30 μm that is too thick to constitute a light emitting diode is used resulting in too long a time taken to grow, and the epitaxial substrate undergoes significant warping after growing. These problems stem from the fact that the nitride semiconductor is grown to a large thickness to obtain a smooth surface, since the surface tends to be rough when the thickness is small.

[0027] While surface smoothness of the light emitting device structure is an important factor in the manufacture of a light emitting device, it has been difficult to form a smooth surface in a light emitting device structure having film thickness of several micrometers that is suitable for. practical application.

[0028] The method described in Applied Physics Letters, Vol. 81 (2002), pp 1201-1203 has such a problem that a significant length of regrowth time is required before the crystal of the regrown GaN layer **134** grows laterally on the mask and meets the adjacent regrown GaN layer **134** thereby to form a smooth surface, while the crystal grows in the direction of thickness as well as in the lateral direction, thus resulting in a large total thickness of the GaN layers. Moreover, the threading dislocations inevitably propagates from the portion of the surface of the regrown GaN layer **134** that is not selectively masked, thus making it difficult to decrease the density of threading dislocations over the entire substrate surface. In addition, since SiO_2 of the mask **133** is embedded in the regrown GaN layer **134**, unintended diffusion of silicon from the mask **133** may cause deterioration in the electric characteristic of the semiconductor device.

[0029] In case nitride semiconductor layers are formed on (01-12)-plane sapphire substrate by the conventional low